IN THE CLAIMS

Please amend the claims as follows:

1.-3. (Canceled)

4. (Previously Presented) A circuit comprising:

a voltage node;

a ground node; and

a transistor including a gate comprising a p-type polysilicon, a gate oxide layer having a thickness of between about 20 angstroms and about 40 angstroms, a drain, and a source, the gate being coupled to the voltage node and the drain and source being coupled to the ground node, the transistor to operate in the depletion mode.

5. (Original) The circuit of claim 4, wherein the operating voltage value is between about .5 volts and about 1.5 volts.

6. (Original) The circuit of claim 5, further comprising:

a logic cell coupled to the voltage node and located in close proximity to the transistor.

7.-8. (Canceled)

9. - 13. (Canceled)

14. (Previously Presented) A circuit comprising:

a die;

a ground node located on the die;

a power supply voltage node located on the die; and

an electronic device having a variable capacitance characteristic and that is permanently coupled between the ground node and the power supply voltage node and capable of providing a removal of charge at a constant rate for an asymmetrical incremental voltage variations about an operational node voltage at the power supply voltage node.

15. (Original) The circuit of claim 14, wherein incremental voltage variations of one polarity are damped and incremental voltage variations of the opposite polarity are amplified.

16. (Previously Presented) The circuit of claim 14, wherein the operational node voltage is about 1.3 volts.

17.-28. (Canceled)

29. (Previously Presented) A circuit comprising:

a voltage node;

a ground node; and

a transistor formed on a silicon-on-sapphire substrate, the transistor including a gate comprising a p-type polysilicon, a gate oxide layer having a thickness of between about 20 angstroms and about 40 angstroms, a drain, and a source, the gate being coupled to the voltage node and the drain and source being coupled to the ground node, the transistor to operate in the depletion mode

30. (Previously Presented) The circuit of claim 29, wherein the gate oxide layer comprises a thermal oxide.

31. (Previously Presented) The circuit of claim 30, further comprising:

a logic cell coupled to the voltage node and located in close proximity to the transistor.

32. (Previously Presented) A circuit comprising:

a gallium arsenide die having a high power supply voltage node and a low power supply voltage node; and

a transistor coupled between the high power supply voltage node and the low power supply voltage node and operable for controlling a voltage at the low power supply voltage node.

33. (Previously Presented) The circuit of claim 32, wherein the transistor has a gate, a drain, and a source, and the gate is coupled to the high power supply voltage node and the source and the drain are coupled to the low power supply voltage node.

34. (Previously Presented) The circuit of claim 33, wherein the transistor includes a gate oxide layer having a thickness of between about 20 angstroms and about 40 angstroms.

35. (Previously Presented) A circuit comprising:

a germanium die;

a ground node located on the germanium die;

a power supply voltage node located on the germanium die; and

an electronic device having a variable capacitance characteristic and that is permanently coupled between the ground node and the power supply voltage node and capable of providing a removal of charge at a constant rate for an asymmetrical incremental voltage variations about an operational node voltage at the power supply voltage node.

36. (Previously Presented) The circuit of claim 35, wherein incremental voltage variations of one polarity are damped and incremental voltage variations of the opposite polarity are amplified.

37. (Previously Presented) The circuit of claim 35, wherein the operational node voltage is about 1.3 volts.